JAMES GARLAND B.Eng. (Hons.), M.Sc. PhD.

Moonstone House, Raheen, Tullow, County Carlow. R93 D952. Ireland.
Home: +353 (0) 59 916 1746 Mobile: +353 (0) 86 173 7766 Email: james@jpgarland.com

Profile

PhD and researcher in Machine Learning in embedded systems. Eleven years of lecturer and supervisor in undergrad and postgrad Electronics. Three years of External Examiner experience. Twenty-one years of industrial experience in design engineering with digital SoC/IP ASIC, FPGA and PCB design, test, training, project management, team lead and customer support experience in various industries.

Publications

- *'Low-precision Logarithmic Number Systems: Beyond Base-2'* - ACM Transactions on Architecture and Code Optimization, 2021. DOI: 10.1145/3461699
- *Many-Core Computing: Hardware and software; 'Chapter 6 Hardware and Software Performance in Deep Learning'* - The Institution of Engineering and Technology, 2019; ISBN: 978-1-78561-582-5
- *'Low Complexity Multiply-Accumulate Units for Convolutional Neural Networks with Weight-Sharing'* - ACM Transactions on Architecture and Code Optimization, 2018; DOI: 10.1145/3233300
- *'Low Complexity Multiply Accumulate Unit for Weight-Sharing Convolutional Neural Networks', - HiPEAC ACACES 2017 Poster Abstracts, 2017, pp. 53-56, ISBN: 978-88-905806-5-9.*
- *'Low Complexity Multiply Accumulate Unit for Weight-Sharing Convolutional Neural Networks'* - IEEE Computer Architecture Letters, 2017; DOI: 10.1109/LCA.2017.2656880

Conferences

- HiPEAC 2019 Paper Session 12: *Low Complexity Multiply-Accumulate Units for Convolutional Neural Networks with Weight-Sharing*
- HiPEAC 2019 Poster Session: *Low Complexity Multiply-Accumulate Units for Convolutional Neural Networks with Weight-Sharing*
- ACACES 2017 Poster Session: *Low Complexity Multiply Accumulate Unit for Weight-Sharing Convolutional Neural Networks*

Qualifications

Ph.D. Computer Science.	Trinity College Dublin, Ireland.	2016-2021
M.Sc. System Design (Microelectronics).	University of Central England, UK.	1995
B.Eng. (Hons.). Engineering (Electrical & Electronic).	Coventry University, UK.	1992-1994
H.N.D. Electrical & Electronic Engineering.	Coventry University, UK.	1990-1992

Career History

Lecturer/Principal Investigator/ Postgrad Supervisor — **Institute of Technology Carlow, Ireland** — **2016 - Present**

- Lecturer in Electronics. Principal investigator/postgrad supervisor of machine learning embedded projects.

Xilinx Open Hardware Judge — **Xilinx Ireland, Ireland** — **2017 - Present**

- Judge for the Annual Xilinx University Program FPGA and SoC University Design Contest.

PhD. Research Candidate — **Trinity College Dublin, Ireland** — **2018 - 2021**

- Researching microarchitectural optimisations of machine learning in FPGA / ASIC / embedded.

PhD. Research Student — **Trinity College Dublin, Ireland** — **2016 - 2018**

- Researching microarchitectural optimisations of machine learning in FPGA / ASIC / embedded.

Staff Software Engineer — **2013 - 2016**

Senior SW & IP Quality Assurance Engineer — **Xilinx Ireland, Ireland** — **2004 - 2013**

- Project managed and technically led testing of both tool flow software & FPGA System IP.
- Trained colleagues in India in EDK IP testing. Trainer for low-cost FPGA design.
- Interviewed and selected new hires in Ireland and India branches. Intern coaching and supervision.

External Examiner — **Institute of Technology Carlow, Ireland** — **2014 - 2016**

- External Examiner for B.Eng. (Hons) and M.Sc. courses in Aero, Mechanical, and Engineering.

Lecturer/Research Supervisor — **Trinity College Dublin, Ireland** — **2003 - 2011**

- Lecturer and project supervisor for the M. Sc. Computer Science (Ubiquitous Computing) Course.

HETAC Review Panel Expert **Institute of Technology Tallaght, Ireland** **2006**

- HETAC review panel member review for two new degree courses to be run at IT Tallaght.

Director/Secretary **Lokico Ltd., Ireland** **2004 - 2006**

- Director, shareholder, and company secretary for a small architectural start-up company.

Lecturer/Research Assistant **Trinity College Dublin, Ireland** **2003 - 2004**

- Lecturer and project supervisor for the M. Sc. Computer Science (Ubiquitous Computing) Course.
- Research assistant designing ARM, FPGA/ASIC system for a Delay Tolerant Sensor Network.
- Proposed an EI Technology Development system for obstruction detection and collision avoidance.

Senior IC Design Engineer **ParthusCeva Inc, Ireland** **1999 - 2002**

- Project managed, technically led, co-designed Bluetooth Verilog Digital IP for FPGA and ASIC with SCAN insertion, STA, and SCAN chain pattern generation. Trained, supported 11 key strategic customers in the use of the IP. Interviewed, selected, and mentored new hires. Fire Officer.

Digital ASIC Designer **ARM Ltd. UK** **1997 - 1999**

- Project manager, team leader, digital ASIC designer digital IP and SoC for the embedded market.

Digital ASIC Designer **LucasVarity, UK** **1995 - 1997**

- Digital ASIC design engineer for the Military, Aerospace, and automotive sectors.

Awards

Xilinx Applications, Development & Verification Solutions World Class Achievement Award. 2009

Relevant Technical Skill Set

Design Packages.	*Simulation*: Synopsys VCS, Mentor ModelSim, Cadence IUS, Xilinx Vivado; *ASIC Synthesis*: Synopsys DCXP, Cadence Genus; *STA*: Synopsys Primetime, Xilinx Vivado, and Trace; *ATPG*: Synopsys Tetramax; *FPGA Synthesis & Implementation*: Xilinx Vivado, Vivado_HLS; *PCB Schematic*: Mentor PowerLogic; *Embedded System Design*: Xilinx IDS (EDK / SDK); Raspberry Pi.
High-Level Languages.	VHDL, Verilog, SystemVerilog, SystemC, C/C++, TCL, Perl, Python.
Low-Level Languages.	Intel, ARM, TMS320c25µP, 8051µC, Z80µP assemblers.

Training Courses

PAISS	PRAIRIE/MIAI AI Summer School.	2021
HiPEAC	HiPEAC Summer School ACACES.	2020
Trinity College Dublin	PG Skills Development Summer School.	2019
IMEC Academy	Hardware-Efficient Machine Learning Summer School.	2019
HiPEAC	HiPEAC Summer School ACACES 2017.	2017
Coursera.org	Machine Learning Specialisation (5 courses).	2017
Trinity College Dublin	Research Methods.	2016
Xilinx Ireland, Ireland	TCL; Python; Perl; Advanced Testing Techniques; Project Management Mastery; Embedded Linux Training for the PowerPC; Facilitative Leadership; Designing With Virtex4 Family; Cadence Incisive Simulation Training; Difficult Conversations; Advanced FPGA Design Techniques.	2004 - 2012
BSM, Ireland.	PACE Core Team Leadership Workshop.	2002
Synopsys, Ireland.	Synopsys DCXP, PrimeTime STA & Tetramax Training.	2002
Bennett, Ireland.	Bennett's Design for Test.	2001
Esperan, Ireland.	Esperan Verilog Course.	2000
Mentor, U. K.	Mentor People Skills Training.	1997 – 1998
ARM, U. K.	ARM Training.	1997

Voluntary Work

Xilinx Ireland.	Judge for the annual Xilinx Open Hardware Competition.
St Columba's National School	IT support.