JAMES GARLAND B.Eng. (Hons.), M.Sc.

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Profile

Researcher in Machine Learning, Software, FPGA & IC Design Engineer with Digital SoC / IP ASIC, FPGA and PCB design and test, training and customer support experience in a variety of different industries. Project manager, team and technical leader. External Examiner, Lecturer and Research Supervisor at a leading Irish University and Institute of Technology. Holds a MSc System Design (Microelectronics), a BEng (Hons) and a HND.

Publications

Low Complexity Multipy Accumulate Unit for Weight-Sharing Convolutional Neural Networks
- Published in IEEE Computer Architecture Letters; DOI: 10.1109/LCA.2017.2656880

Career History

Lecturer **IT Carlow, Carlow, Ireland.** **2016 - Present**
- Lecturer in Digital Electronics and Communications Systems.

PhD Research Student **Trinity College Dublin, Ireland.** **2016 - Present**
- Researching machine learning implementations in FPGA.

Staff Software Engineer. **2013 - 2016**
Senior SW & IP Quality Assurance Engineer. **Xilinx Ireland, Dublin, Ireland.** **2004 - 2013**
- Project managed, technically led testing of both tool flow software & FPGA System IP targeted at the ARM, PowerPC and MicroBlaze processors on Xilinx FPGAs and hardware platforms.
- Trained colleagues in India in EDK IP testing. Trainer for low cost FPGA design.
- Interviewed and selected recruitment candidates in Ireland and India branches.
- Intern coaching and supervision.

External Examiner. **Institute of Technology, Carlow, Ireland.** **2014 - 2016**
- External Examiner for B.Eng. (Hons) and M.Sc. courses in Aero, Mechanical and Engineering.

Lecturer/Research Supervisor. **Trinity College Dublin, Dublin, Ireland.** **2003 - 2011**
- Lecturer / research and project supervisor in Embedded Hardware Design for a M.Sc. Computer Science Course. Periodic undergraduate student supervisor.

HETAC Review Panel Expert. **IT Tallaght, Dublin, Ireland.** **2006**
- Sat on the HETAC review panel to review 2 new degree courses to be run at IT Tallaght.

Director/Shareholder/Secretary. **Lokico Ltd., Ireland.** **2004 - 2006**
- Director, shareholder and company secretary for a small start-up company producing architectural plans and assisting in obtaining planning permission for one-off Irish housing.

Lecturer/Research Assistant. **Trinity College Dublin, Dublin, Ireland.** **2003 - 2004**
- Lecturer and project supervisor in Embedded Hardware Design for the M. Sc. Computer Science (Ubiquitous Computing) Course.
- Research assistant specifying, designing and testing ARM / Xscale, FPGA / ASIC hardware in Verilog, PCB schematic and software drivers for a Delay Tolerant Sensor Network.
- Proposed, specifying, designing and testing an EI Technology Development funded sensor system for obstruction detection and collision avoidance for smart roads.

Senior IC Design Engineer. **ParthusCeva Inc., Dublin, Ireland.** **1999 - 2002**
- Project managed, specified, technically led and co-designed and tested in FPGA Bluetooth Verilog Digital IP for ASIC with SCAN insertion, STA and SCAN chain pattern generation.
- Trained and supported up to 11 key & strategic customers on and off site in the use of the IP.
- Interviewed, selected and mentored recruitment candidates. Fire Officer.

Digital ASIC Designer. **ARM Ltd., Cambridge. U.K.** **1997 - 1999**
- Project manager, team leader, digital ASIC designer digital IP and SoC for the embedded market.

Digital ASIC Designer. **LucasVarity, Birmingham, U.K.** **1995 - 1997**
- Digital ASIC design engineer for the Military, Aerospace and automotive sectors.

Qualifications

M. Sc. System Design (Microelectronics).	Birmingham City University (nee UCE), Birmingham, U.K.	1995
B. Eng. (Hons.). Engineering (Electrical & Electronic).	Coventry University. U.K.	1992-1994
H. N. D. Electrical & Electronic Engineering.	Coventry University. U.K.	1990-1992

Awards

Xilinx Applications, Development & Verification Solutions World Class Achievement Award. 2009

Relevant Technical Skill Set

Design Packages.	**Simulation:** Synopsys VCS, MTI ModelSim, Cadence IUS, Vantage Compiler & Simulator, Xilinx Vivado Simulator; **ASIC Synthesis:** Synopsys DCXP; Cadence Genus; **STA:** Synopsys Primetime, Xilinx Trace; Xilinx Vivado; **ATPG:** Synopsys Tetramax; **FPGA Synthesis:** Altera MaxPlus II, Exemplar Leonardo Spectrum for Altera, Xilinx IDS (XST), Xilinx Vivado, Xilinx Vivado_HLS; **FPGA Implementation:** Altera Quartus, Xilinx IDS, Xilinx Vivado; **PCB Schematic:** Mentor PowerLogic; **Embedded System Design:** Xilinx IDS (EDK / SDK); Raspberry Pi.
High Level Languages.	VHDL, Verilog, SystemVerilog, SystemC, TCL, Perl, Python, Shell Scripts, Pascal, C, BASIC.
Low Level Languages.	Assemblers for: ARM, TMS320c25µP, 8051µC, Z80 µP.

Relevant Work Related Training Courses

HiPEAC	HiPEAC Summer School ACACES 2017.	2017
Coursera.org	Machine Learning Specialisation.	2017
Xilinx Ireland, Ireland	TCL and Python.	2012
Xilinx Ireland, Ireland	Advanced Testing Techniques.	2010
Xilinx Ireland, Ireland	Project Management Mastery.	2009
Xilinx Ireland, Ireland	Embedded Linux Training for the PowerPC. Facilitative Leadership.	2006
Xilinx Ireland, Ireland	Designing With the Virtex4 Family. Cadence Incisive Simulation Training. Difficult Conversations.	2005
Xilinx Ireland, Ireland	Advanced FPGA Design Techniques (EDK / ISE); Perl.	2004
BSM, Ireland.	PACE Core Team Leadership Workshop.	2002
Synopsys, Ireland.	Synopsys DCXP, PrimeTime STA & Tetramax Training.	2002
Bennett, Ireland.	Bennett's Design For Test.	2001
Esperan, Ireland.	Esperan Verilog Course.	2000
Mentor, U. K.	Mentor People Skills Training.	1997 – 1998
ARM, U. K.	ARM Training.	1997

Personal Details

Marital Status.	Married, 1 son, 1 daughter.
Interests.	Music, 'Cello, Guitar, Mandolin, Ukulele, Cycling, Badminton, Swimming, Photography, Videography, Hiking, Computers, General & Technical Reading.
Other Details.	Holder of Full Clean E.U. Driving Licence.