JAMES GARLAND **BEng (Hons), MSc, PhD**

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Profile

Lecturer and principal investigator researching the micro-architectural implementations and robotic applications of deep learning algorithms in FPGA, ASIC and embedded systems. Thirteen years of lecturing and supervising in undergraduate and postgraduate electronics. Three years as an external examiner. Twenty-one years of industrial experience in diverse industries in SoC/IP ASIC, FPGA, and PCB design, test, training, project management, team lead, and customer support.

Publications

- *'Laser Beam Propagation Features via Atmospheric Turbulence-Induced Beam Wander: Testbed Conceptual Design'* - Communications and Observations through Atmospheric Turbulence (COAT), 2023. URI: https://hal.science/hal-04246206.
- *'Spatial Mapping of light aircraft with stereo-vision camera for use on Unmanned Aircraft System for defect localisation'* - 2023 International Conference on Unmanned Aircraft Systems (ICUAS). DOI: 10.1109/icuas57906.2023.10155987.
- *'Feature Representation in Pretrained Deep Metric Embeddings'* - Research Square Platform LLC, 2023. DOI: 10.21203/rs.3.rs-2761696/v1.
- *'Arbitrary Precision and Low Complexity Micro-Architectural Arithmetic Optimisations of Machine Learning Algorithms for Compute Bound and High-Performance Systems',* - PhD Thesis, Trinity College Dublin. School of Computer Science & Statistics, 2021.
- *'Low-precision Logarithmic Number Systems: Beyond Base-2'* - ACM Transactions on Architecture and Code Optimization, 2021. DOI: 10.1145/3461699.
- *Many-Core Computing: Hardware and software; 'Chapter 6 Hardware and Software Performance in Deep Learning'* - The Institution of Engineering and Technology, 2019; ISBN: 978-1-78561-582-5.
- *'Low Complexity Multiply-Accumulate Units for Convolutional Neural Networks with Weight-Sharing'* - ACM Transactions on Architecture and Code Optimization, 2018; DOI: 10.1145/3233300.
- *'Low Complexity Multiply Accumulate Unit for Weight-Sharing Convolutional Neural Networks'*, - HiPEAC ACACES 2017 Poster Abstracts, 2017, pp. 53-56, ISBN: 978-88-905806-5-9.
- *'Low Complexity Multiply Accumulate Unit for Weight-Sharing Convolutional Neural Networks'* - IEEE Computer Architecture Letters, 2017; DOI: 10.1109/LCA.2017.2656880.

Conferences

- Communications and Observations through Atmospheric Turbulence (COAT) Workshop 2023: *'Laser Beam Propagation Features via Atmospheric Turbulence-Induced Beam Wander: Testbed Conceptual Design.'*
- 21st Workshop on Compilers for Parallel Computing (CPC) 2021: *'HOBFLOPS CNNs: Hardware Optimized Bitslice-Parallel Floating-Point Operations for Convolutional Neural Networks.'*
- HiPEAC 2019 Paper Session 12: *'Low Complexity Multiply-Accumulate Units for Convolutional Neural Networks with Weight-Sharing.'*
- HiPEAC 2019 Poster Session: *'Low Complexity Multiply-Accumulate Units for Convolutional Neural Networks with Weight-Sharing.'*
- ACACES 2017 Poster Session: *'Low Complexity Multiply Accumulate Unit for Weight-Sharing Convolutional Neural Networks.'*

Qualifications

PhD Computer Science.	Trinity College Dublin, Ireland.	2016 - 2021
MSc System Design (Microelectronics).	University of Central England, UK.	1994 - 1995
BEng (Hons) Engineering (Electrical & Electronic).	Coventry University, UK.	1992 - 1994
HND Electrical & Electronic Engineering.	Coventry University, UK.	1990 - 1992

Professional Activities

AMD Xilinx Open Hardware Design Competition Judge.	2017 - Present
St Columba's National School, IT support. Robotics Teaching.	2016 - Present
Two nominations for the Supervisor Award under the SETU Research Excellence Awards.	2022
Xilinx Applications, Development & Verification Solutions World Class Achievement Award.	2009

J A M E S G A R L A N D BEng (Hons), MSc, PhD

Career History

Lecturer/Principal Investigator (PI)/ Postgrad Advisor — **South East Technological University, Ireland** — 2016 - Present

Lecturer in Electronics. PI, Master's and PhD advisor of robotic and machine learning embedded projects.

Engineers Ireland Review Panel Expert — **Technological University Dublin, Ireland** — 2023

Engineers Ireland review panel member review for two new degree courses to be run at TU Dublin.

Xilinx Open Hardware Judge — **Xilinx Ireland, Ireland** — 2017 - Present

Judge for the Annual Xilinx University Program FPGA and SoC University Design Contest.

PhD Research Candidate — **Trinity College Dublin, Ireland** — 2018 - 2021

Researching microarchitectural optimisations of machine learning in FPGA / ASIC / embedded.

PhD Research Student — **Trinity College Dublin, Ireland** — 2016 - 2018

Researching microarchitectural optimisations of machine learning in FPGA / ASIC / embedded.

Staff Software Engineer — 2013 - 2016

Senior SW & IP Quality Assurance Engineer — **Xilinx Ireland, Ireland** — 2004 - 2013

Project managed and technically led testing of tool flow software and FPGA System IP.
Trained colleagues in India in EDK IP testing. Trainer for low-cost FPGA design.
Interviewed and selected new hires in Ireland and India branches. Intern coaching and supervision.

External Examiner — **Institute of Technology Carlow, Ireland** — 2014 - 2016

External Examiner for B.Eng. (Hons) and M.Sc. courses in Aero, Mechanical, and Engineering.

Lecturer/Research Supervisor — **Trinity College Dublin, Ireland** — 2003 - 2011

Lecturer and project supervisor for the M. Sc. Computer Science (Ubiquitous Computing) Course.

HETAC Review Panel Expert — **Institute of Technology Tallaght, Ireland** — 2006

HETAC review panel member review for two new degree courses to be run at IT Tallaght.

Director/Secretary — **Lokico Ltd., Ireland** — 2004 - 2006

Director, shareholder, and company secretary for a small architectural start-up company.

Lecturer/Research Assistant — **Trinity College Dublin, Ireland** — 2003 - 2004

Lecturer and project supervisor for the M. Sc. Computer Science (Ubiquitous Computing) Course.
Research assistant designing ARM, FPGA/ASIC system for a Delay Tolerant Sensor Network.
Proposed an EI Technology Development system for obstruction detection and collision avoidance.

Senior IC Design Engineer — **ParthusCeva Inc, Ireland** — 1999 - 2002

Project managed, technically led, and co-designed Bluetooth Verilog Digital IP for FPGA and ASIC with SCAN insertion, STA, and SCAN chain pattern generation. Trained and supported 11 critical strategic customers in using the IP. Interviewed, selected, and mentored new hires. Fire Officer.

Digital ASIC Designer — **ARM Ltd. UK** — 1997 - 1999

Project manager, team leader, digital ASIC designer, digital IP and SoC for the embedded market.

Digital ASIC Designer — **LucasVarity, UK** — 1995 - 1997

Digital ASIC design engineer for the Military, Aerospace, and automotive sectors.

Training Courses

PAISS	PRAIRIE/MIAI AI Summer School.	2021
HiPEAC	HiPEAC Summer School ACACES.	2020
Trinity College Dublin	PG Skills Development Summer School.	2019
IMEC Academy	Hardware-Efficient Machine Learning Summer School.	2019
HiPEAC	HiPEAC Summer School ACACES 2017.	2017
Coursera.org	Machine Learning Specialisation (5 courses).	2017
Trinity College Dublin	Research Methods.	2016
Xilinx Ireland, Ireland	TCL; Python; Perl; Advanced Testing Techniques; Project Management Mastery; PowerPC Embedded Linux Training; Facilitative Leadership; Cadence Incisive Simulation Training; Difficult Conversations; Advanced FPGA Design.	2004 - 2012
BSM, Ireland.	PACE Core Team Leadership Workshop.	2002
Synopsys, Ireland.	Synopsys DCXP, PrimeTime STA, Tetramax Training.	2002
Bennett, Ireland.	Bennett's Design for Test.	2001
Esperan, Ireland.	Esperan Verilog Course.	2000
Mentor, U. K.	Mentor People Skills Training.	1997 - 1998
ARM, U. K.	ARM Training.	1997